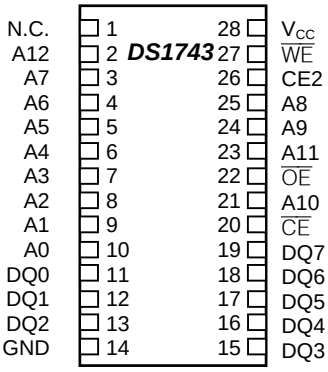
DS1743/DS1743P
Y2K-Compliant, Nonvolatile Timekeeping RAMs

FEATURES

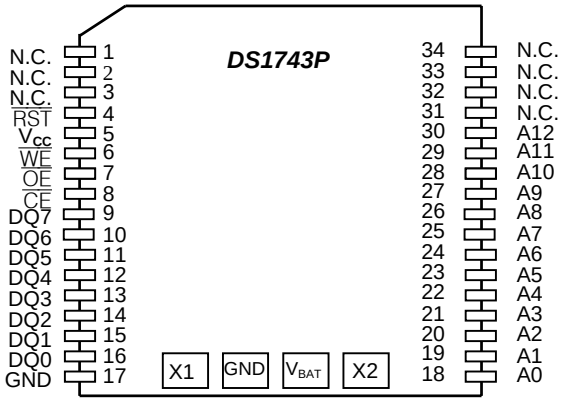
- Integrated NV SRAM, Real-Time Clock, Crystal, Power-Fail Control Circuit, and Lithium Energy Source
- Clock Registers are Accessed Identically to the Static RAM. These Registers Reside in the Eight Top RAM Locations.
- Century Byte Register
- Totally Nonvolatile with Over 10 Years of Operation in the Absence of Power
- BCD-Coded Century, Year, Month, Date, Day, Hours, Minutes, and Seconds with Automatic Leap Year Compensation Valid through 2099
- Low-Battery-Voltage Level Indicator Flag
- Power-Fail Write Protection Allows for ±10% V_{CC} Power-Supply Tolerance
- Lithium Energy Source is Electrically Disconnected to Retain Freshness Until Power is Applied for the First Time
- DIP Module Only
  Standard JEDEC Bytewide 8k x 8 Static RAM Pinout
- PowerCap Module Board Only
  Surface-Mountable Package for Direct Connection to PowerCap Containing Battery and Crystal
  Replaceable Battery (PowerCap)
  Power-On Reset Output
  Pin-for-Pin Compatible with Other Densities of DS174XP Timekeeping RAM
- Underwriters Laboratories (UL) Recognized to Prevent Charging of the Internal Lithium Battery

PIN CONFIGURATIONS

TOP VIEW



28-Pin Encapsulated Package
(28 PIN 740)



34-Pin PowerCap Module Board
(Uses DS9034PCX PowerCap)

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE	VOLTAGE (V)	TOP MARK**
DS1743-85	0°C to +70°C	28 EDIP Module	5	DS1743-85
DS1743-100	0°C to +70°C	28 EDIP Module	5	DS1743-100
DS1743-100 IND	-40°C to +85°C	28 EDIP Module	5	DS1743-100-IND
DS1743P-85	0°C to +70°C	34 PowerCap*	5	DS1743P-85
DS1743P-100	0°C to +70°C	34 PowerCap*	5	DS1743P-100
DS1743P-100IND	-40°C to +85°C	34 PowerCap*	5	DS1743P-100 IND
DS1743W-120	0°C to +70°C	28 EDIP Module	3.3	DS1743W-120
DS1743W-120 IND	-40°C to +85°C	28 EDIP Module	3.3	DS1743W-120 IND
DS1743W-150	0°C to +70°C	28 EDIP Module	3.3	DS1743W-150
DS1743W-150 IND	-40°C to +85°C	28 EDIP Module	3.3	DS1743W-150 IND
DS1743WP-120	0°C to +70°C	34 PowerCap*	3.3	DS1743WP-120
DS1743WP-120 IND	-40°C to +85°C	34 PowerCap*	3.3	DS1743WP-120 IND
DS1743-85+	0°C to +70°C	28 EDIP Module	5	DS1743-85
DS1743-100+	0°C to +70°C	28 EDIP Module	5	DS1743-100
DS1743-100 IND+	-40°C to +85°C	28 EDIP Module	5	DS1743-100-IND
DS1743P-85+	0°C to +70°C	34 PowerCap*	5	DS1743P-85
DS1743P-100+	0°C to +70°C	34 PowerCap*	5	DS1743P-100
DS1743P-100IND+	-40°C to +85°C	34 PowerCap*	5	DS1743P-100 IND
DS1743W-120+	0°C to +70°C	28 EDIP Module	3.3	DS1743W-120
DS1743W-120 IND+	-40°C to +85°C	28 EDIP Module	3.3	DS1743W-120 IND
DS1743W-150+	0°C to +70°C	28 EDIP Module	3.3	DS1743W-150
DS1743W-150 IND+	-40°C to +85°C	28 EDIP Module	3.3	DS1743W-150 IND
DS1743WP-120+	0°C to +70°C	34 PowerCap*	3.3	DS1743WP-120
DS1743WP-120 IND+	-40°C to +85°C	34 PowerCap*	3.3	DS1743WP-120 IND
DS9034PCX	0°C to +70°C	PowerCap	—	DS9034PC
DS9034I-PCX	-40°C to +85°C	PowerCap IND	—	DS9034PCI
DS9034PCX+	0°C to +70°C	PowerCap	—	DS9034PC
DS9034I-PCX+	-40°C to +85°C	PowerCap IND	—	DS9034PCI

+Denotes a lead-free package.
**DS9034PCX required (must be ordered separately).*
***A '+' indicates lead-free. The top mark will include a '+' symbol on lead-free devices.*

DESCRIPTION

The DS1743 is a full-function, year-2000-compliant (Y2KC), real-time clock/calendar (RTC) and 8k x 8 nonvolatile static RAM. User access to all registers within the DS1743 is accomplished with a bytewide interface as shown in Figure 1. The RTC information and control bits reside in the eight uppermost RAM locations. The RTC registers contain century, year, month, date, day, hours, minutes, and seconds data in 24-hour binary-coded decimal (BCD) format. Corrections for the day of the month and leap year are made automatically. The RTC clock registers are double buffered to avoid access of incorrect data that can occur during clock update cycles. The double-buffered system also prevents time loss as the timekeeping countdown continues unabated by access to time register data. The DS1743 also contains its own power-fail circuitry, which deselects the device when the V_{CC} supply is in an out-of-tolerance condition. When V_{CC} is above V_{PF}, the device is fully accessible. When V_{CC} is below V_{PF}, the internal $\overline{CE}$ signal is forced high, preventing any access. When V_{CC} rises above V_{PF}, access remains inhibited for T_{REC}, allowing time for the system to stabilize. These features prevent loss of data from unpredictable system operation brought on by low V_{CC} as errant access and update cycles are avoided.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……-0.3V to +6.0V
Operating Temperature Range……-40°C to +85°C
Storage Temperature Range……-40°C to +85°C
Soldering Temperature (EDIP) (leads, 10 seconds)……..…+260°C
Soldering Temperature……..….See J-STD-020 Specification (See Note 8)

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMP RANGE	V_{CC}
Commercial	0°C to +70°C	3.3V ±10% or 5V ±10%
Industrial	-40°C to +85°C	3.3V ±10% or 5V ±10%

RECOMMENDED DC OPERATING CONDITIONS

(T_A = Over the Operating Range.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Logic 1 Voltage All Inputs	V_{IH}	V_{CC} = 5V ±10%	2.2		V_{CC} +0.3V	V	1
		V_{CC} = 3.3V ±10%	2.0		V_{CC} +0.3V	V	1
Logic 0 Voltage All Inputs	V_{IL}	V_{CC} = 5V ±10%	-0.3		+0.8	V	1
		V_{CC} = 3.3V ±10%	-0.3		+0.6	V	1

DC ELECTRICAL CHARACTERISTICS (5V)

(V_{CC} = 5.0V ±10%, T_A = Over the Operating Range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	I_{CC}		15	50	mA	2, 3
TTL Standby Current ($\overline{CE}$ = V_{IH}, CE2 = V_{IL})	I_{CC1}		1	3	mA	2, 3
CMOS Standby Current ($\overline{CE} \geq V_{CC}$ - 0.2V; CE2 = GND + 0.2V)	I_{CC2}		1	3	mA	2, 3
Input Leakage Current (Any Input)	I_{IL}	-1		+1	µA	
Output Leakage Current (Any Output)	I_{OL}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0mA)	V_{OH}	2.4				1
Output Logic 0 Voltage (I_{OUT} = 2.1mA)	V_{OL1}			0.4		1
Write-Protection Voltage	V_{PF}	4.20		4.50	V	1
Battery Switchover Voltage	V_{SO}		V_{BAT}			1, 4

DC ELECTRICAL CHARACTERISTICS (3.3V)

(V_{CC} = **3.3V ±10%**, T_A = Over the Operating Range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	I_{CC}		10	30	mA	2, 3
TTL Standby Current ($\overline{CE}$ = V_{IH})	I_{CC1}		0.7	2	mA	2, 3
CMOS Standby Current ($\overline{CE}$ ≥ V_{CC} - 0.2V; CE2 = GND + 0.2V)	I_{CC2}		0.7	2	mA	2, 3
Input Leakage Current (Any Input)	I_{IL}	-1		+1	µA	
Output Leakage Current (Any Output)	I_{OL}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0mA)	V_{OH}	2.4				1
Output Logic 0 Voltage (I_{OUT} =2.1mA)	V_{OL1}			0.4		1
Write-Protection Voltage	V_{PF}	2.75		2.97	V	1
Battery Switchover Voltage	V_{SO}		V_{BAT} or V_{PF}		V	1, 4

AC CHARACTERISTICS—READ CYCLE (5V)

(V_{CC} = 5.0V ±10%, T_A = Over the Operating Range.)

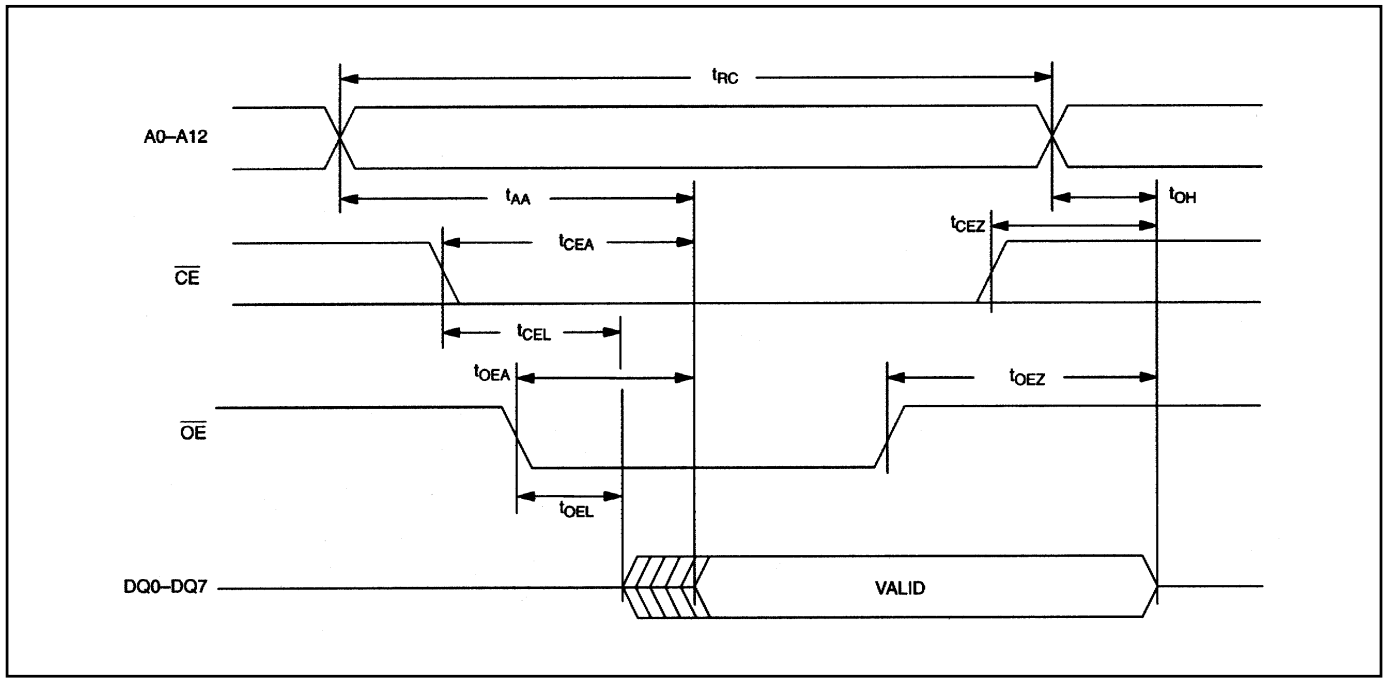
PARAMETER	SYMBOL	ACCESS						UNITS	NOTES
		70ns		85ns		100ns			
		MIN	MAX	MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	70		85		100		ns	
Address Access Time	t_{AA}		70		85		100	ns	
$\overline{CE}$ to CE2 to DQ Low-Z	t_{CEL}	5		5		5		ns	5
$\overline{CE}$ Access Time	t_{CEA}		70		85		100	ns	5
CE2 Access Time	t_{CE2A}		80		95		105	ns	5
$\overline{CE}$ and CE2 Data-Off Time	t_{CEZ}		25		30		35	ns	
$\overline{OE}$ to DQ Low-Z	t_{OEL}	5		5		5		ns	
$\overline{OE}$ Access Time	t_{OEA}		35		45		55	ns	
$\overline{OE}$ Data-Off Time	t_{OEZ}		25		30		35	ns	
Output Hold from Address	t_{OH}	5		5		5		ns	

AC CHARACTERISTICS—READ CYCLE (3.3V)

(V_{CC} **= 3.3V ±10%**, T_A = Over the Operating Range.)

PARAMETER	SYMBOL	ACCESS				UNITS	NOTES
		120ns		150ns			
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	120		150		ns	
Address Access Time	t_{AA}		120		150	ns	
$\overline{CE}$ and CE2 Low to DQ Low-Z	t_{CEL}	5		5		ns	5
$\overline{CE}$ and CE2 Access Time	t_{CEA}		120		150	ns	5
$\overline{CE}$ and CE2 Data-Off time	t_{CEZ}		40		50	ns	5
$\overline{OE}$ Low to DQ Low-Z	t_{OEL}	5		5		ns	
$\overline{OE}$ Access Time	t_{OEA}		100		130	ns	
$\overline{OE}$ Data-Off Time	t_{OEZ}		35		35	ns	
Output Hold from Address	t_{OH}	5		5		ns	

READ CYCLE TIMING DIAGRAM



AC CHARACTERISTICS—WRITE CYCLE (5V)

(V_{CC} = 5.0V ±10%, T_A = Over the Operating Range.)

PARAMETER	SYMBOL	ACCESS						UNITS	NOTES
		70ns		85ns		100ns			
		MIN	MAX	MIN	MAX	MIN	MAX		
Write Cycle Time	t_{WC}	70		85		100		ns	
Address Setup Time	t_{AS}	0		0		0		ns	5
$\overline{WE}$ Pulse Width	t_{WEW}	50		65		70		ns	
$\overline{CE}$ Pulse Width	t_{CEW}	60		70		75		ns	5
CE2 Pulse Width	t_{CE2W}	65		75		85		ns	5
Data Setup Time	t_{DS}	30		35		40		ns	5
Data Hold Time $\overline{CE}$	t_{DH}	0		0		0		ns	5
Data Hold Time CE2	t_{DH}	8		8		8		ns	5
Address Hold Time	t_{AH}	5		5		5		ns	5
$\overline{WE}$ Data-Off Time	t_{WEZ}		25		30		35	ns	
Write Recovery Time	t_{WR}	10		10		10		ns	

AC CHARACTERISTICS—WRITE CYCLE (3.3V)

(**V_{CC} = 3.3V ±10%**, T_A = Over the Operating Range.)

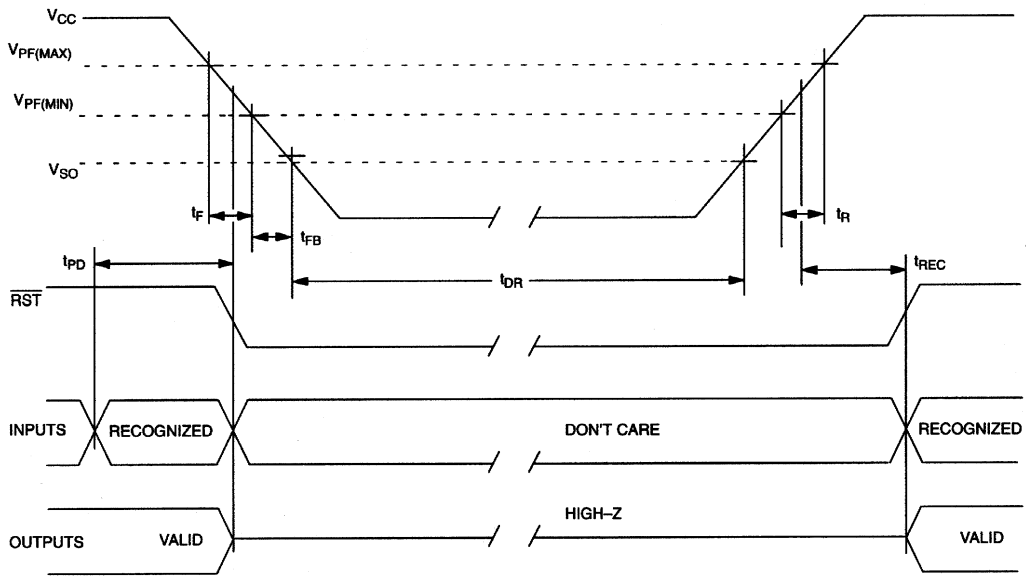
PARAMETER	SYMBOL	ACCESS				UNITS	NOTES
		120ns		150ns			
		MIN	MAX	MIN	MAX		
Write Cycle Time	t_{WC}	120		150		ns	
Address Setup Time	t_{AS}	0		0		ns	5
$\overline{WE}$ Pulse Width	t_{WEW}	100		130		ns	
$\overline{CE}$ and CE2 Pulse Width	t_{CEW}	110		140		ns	5
Data Setup Time	t_{DS}	80		90		ns	5
Data Hold Time $\overline{CE}$	t_{DH}	0		0		ns	5
Data Hold Time CE2	t_{DH}	10		10		ns	5
Address Hold Time	t_{AH}	0		0		ns	5
$\overline{WE}$ Data-Off Time	t_{WEZ}		40		50	ns	
Write Recovery Time	t_{WR}	10		10		ns	

POWER-UP/DOWN CHARACTERISTICS—5V

(V_{CC} = 5.0V ±10%, T_A = Over the Operating Range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at V_{IH}, CE2 at V_{IL}, Before Power-Down	t_{PD}	0			µs	
V_{CC} Fall Time: $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_F	300			µs	
V_{CC} Fall Time: $V_{PF(MIN)}$ to V_{SO}	t_{FB}	10			µs	
V_{CC} Rise Time: $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_R	0			µs	
Power-Up Recover Time	t_{REC}			35	ms	
Expected Data-Retention Time (Oscillator On)	t_{DR}	10			years	6, 7

POWER-UP/DOWN TIMING (5V DEVICE)

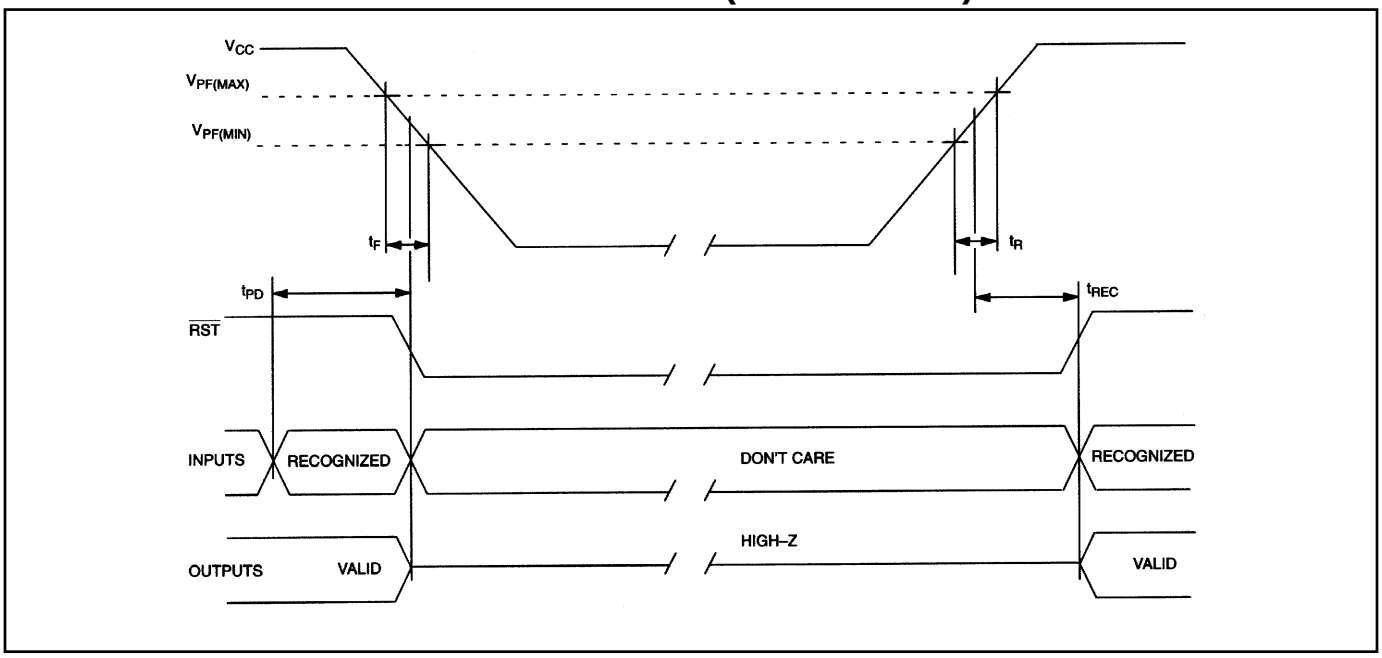


POWER-UP/DOWN CHARACTERISTICS—3.3V

(V_{CC} **= 3.3V ±10%**, T_A = Over the Operating Range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at V_{IH}, Before Power-Down	t_{PD}	0			µs	
V_{CC} Fall Time: $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_F	300			µs	
V_{CC} Rise Time: $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_R	0			µs	
V_{PF} to $\overline{RST}$ High	t_{REC}			35	ms	
Expected Data-Retention Time (Oscillator On)	t_{DR}	10			years	6, 7

POWER-UP/DOWN WAVEFORM TIMING (3.3V DEVICE)



CAPACITANCE

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance on All Input Pins	C_{IN}			7	pF	
Capacitance on All Output Pins	C_O			10	pF	

AC TEST CONDITIONS

Output Load: 50 pF + 1TTL Gate
Input Pulse Levels: 0 to 3.0V
Timing Measurement Reference Levels:
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

NOTES:

1) Voltages are referenced to ground.
2) Typical values are at +25°C and nominal supplies.
3) Outputs are open.
4) Battery switchover occurs at the lower of either the battery terminal voltage or V_{PF}.
5) The CE2 control signal functions the same as the $\overline{CE}$ signal except that the logic levels for active and inactive levels are opposite. If CE2 is used to terminate a write, the CE2 data hold time (t_{DH}) applies.
6) Data-retention time is at +25°C.
7) Each DS1743 has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined for DIP modules as a cumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
8) RTC Encapsulated DIP Modules (EDIP) can be successfully processed through conventional wave-soldering techniques as long as temperatures as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. Post-solder cleaning with water-washing techniques is acceptable, provided that ultrasonic vibration is not used. See the PowerCap package drawing for details regarding the PowerCap package.